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(54) SILICON SINGLE CRYSTAL WAFER AND ITS PRODUCTION

(57)Abstract:
PROBLEM TO BE SOLVED: To produce using CZ method under stable conditions a silicon single crystal wafer having OSF or OSF nuclei on the whole crystal surface or the whole crystal surface except the outer peripheral part when subjected to thermal oxidation treatment and having gettering ability as well.
SOLUTION: This silicon single crystal wafer is produced according to the following procedure: during crystal growth process, the in-oven temperature of a production unit used is controlled in such a manner that ΔG stands at ≤ 0 when ΔG is defined as: $\Delta G=(Ge-Gc)$ [G is the temperature gradient between the crystal melting point and 1,400°C in the vicinity of the solid-liquid interface in the crystal (magnitude of temperature change/length in the direction of crystal axis) (°C/cm); Gc is the temperature gradient at the central part of the crystal; Ge is the temperature gradient of the peripheral part of the crystal], and the resulting single crystal is pulled up under control within the range between the pull-up rate corresponding to the minimum value of the inside line of OSF region and that corresponding to the maximum value of the outside line of the OSF region when the OSF region represents band-like inverse M shape or U-shape in the diagram showing crystal defect distribution with crystal diameter as abscissa and pull-up rate as ordinate.

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CLAIMS

[Claim(s)]
[Claim 1] The silicon single crystal wafer which is a silicon single crystal wafer raised by the Czochrlski method, and is characterized by the nucleus of OSF or OSF existing in the whole crystal surface or the whole surface except the periphery section when thermal oxidation processing is carried out.
[Claim 2] The silicon single crystal wafer which is a silicon single crystal wafer raised by the Czochrlski method, and is characterized by the nucleus of OSF or OSF existing in 90% or more of area of the whole wafer surface when thermal oxidation processing is carried out.
[Claim 3] The silicon single crystal wafer which is a silicon single crystal wafer indicated to said claim 1 or claim 2, and is characterized by FPD, COP, and ratio of length to diameter not existing in the whole wafer surface.
[Claim 4] The silicon single crystal wafer indicated in any 1 term of claim 1 characterized by the oxygen density of said wafer being less than 24 ppmas thru/or claim 3.
[Claim 5] The consistency of OSF generated when said thermal oxidation processing is carried out is 2 100 pieces/cm. Silicon single crystal wafer indicated in any 1 term of claim 1 characterized by being the following thru/or claim 4.
[Claim 6] The epitaxial wafer characterized by using as a substrate the silicon single crystal wafer indicated to claim 1 thru/or claim 5.
[Claim 7] [when manufacturing a silicon single crystal with the Czochrlski method] The silicon single crystal raised sets the temperature gradient between 1400 degrees C to G (the amount of temperature changes / crystal orientation die length) [**/cm] from the melting point near [under crystal] the solid-liquid interface at the time of crystal growth. When the difference of the temperature gradient Gc of a crystal center part [**/cm] and the temperature gradient germanium of a crystal circumference part [**/cm] is expressed with **G= (germanium-Gc), so that **G may become 0 or negative In the defective distribution map in which having controlled whenever [furnace temperature / of the equipment to be used], and having set the axis of abscissa the axis of ordinate as the crystal diameter as the pull-up rate, and having shown defective distribution The manufacture approach of the silicon single crystal characterized by pulling up a crystal, controlling within the limits of the pull-up rate corresponding to the minimum value of the inside line of an OSF field, and the pull-up rate corresponding to the maximum of the outside line of an OSF field when an OSF field forms band-like reverse the mold of M characters or, and a U character mold.
[Claim 8] MCZ which impresses a magnetic field when manufacturing the silicon single crystal by said Czochrlski method -- the manufacture approach of the silicon single crystal indicated to claim 7 characterized by using law.
[Claim 9] said MCZ -- the manufacture approach of the silicon single crystal indicated to claim 8 characterized by impressing the magnetic field of 2000 or more Gausses in a horizontal magnetic field when manufacturing the silicon single crystal by law.
[Claim 10] The manufacture approach of the silicon single crystal indicated in any 1 term of claim 7 characterized by making precision of the pull-up rate at the time of said crystal growth less than into the average**0.01 of the pull-up rate computed for every growth die length of 10cm of a crystal standard diameter portion [mm/min] thru/or claim 9.
[Claim 11] The manufacture approach of the silicon single crystal indicated in any 1 term of claim 7 characterized by preparing an annular solid-liquid interface heat insulator in pull-up equipment, and setting

spacing on this and the front face of melt as 5-10cm in order to control whenever [said furnace temperature] thru/or claim 10.
[Claim 12] The manufacture approach of the epitaxial wafer characterized by growing up an epitaxial layer by using as a substrate the silicon single crystal wafer obtained from the silicon single crystal obtained by the approach of claim 7 thru/or claim 11.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention has few crystal defects and it is related with the silicon single crystal wafer equipped with gettering capacity, and its manufacture approach.
[0002]
[Description of the Prior Art] In recent years, the quality demand to the silicon single crystal produced with the Czochrlski method (it is hereafter written as a CZ process) used as the substrate has been increasing with detailed-izing of the component accompanying high integration of a semiconductor circuit. The defect of a single crystal growth reason in which the oxide film proof-pressure property especially called grown-in (Grown-in) defects, such as FPD, LSTD, and COP, and the property of a device are worsened exists, and importance is attached to reduction of the consistency and size.
[0003] In explaining these defects, it explains being known generally about the factor which determines each concentration of the point defect of the hole mold first called the Vacancy (it may outline Vacancy and Following V) incorporated by the silicon single crystal, and the mold silicon point defect between grids called Interstitial-Si (it may outline Interstitial-Si and Following I) incorporated.
[0004] In a silicon single crystal, V fields are Vacancy, i.e., the crevice generated from lack of a silicon atom, and a field with many things like a hole. With an I region It is the thing of a field with many lumps of the rearrangement and the excessive silicon atom which are generated when a silicon atom exists in an excess. Between V field and an I region The neutral (it may outline Neutral and Following N) field without lack of an atom or an excess (few) will exist. And with [even if said grown-in defects (FPD, LSTD, COP, etc.) occur when V and I are in a condition / ****** / to the last, and it has the bias of some atoms] saturation [below], it has turned out that it does not exist as a defect.
[0005] The concentration of both this point defect is decided from the pull-up rate (growth rate) of the crystal in a CZ process, and relation with the temperature gradient G near [under crystal] the solid-liquid interface. The defect called OSF (an oxidation induction stacking fault, Oxidation Indused Stacking Fault) near [boundary] V field and an I region When it sees in the cross section of the perpendicular direction to a crystal growth shaft, being distributed in the shape of a ring (it being hereafter called an OSF ring) is checked.
[0006] The defect of these crystal growth reason is acquired as a defective distribution map as shown in drawing 5 , when a crystal orientation changes a growth rate from a high speed to a low speed with CZ pull-up machine with which the temperature gradient G near the solid-liquid interface used the large structure in a furnace (hot zone: it may be called HZ) during the usual crystal.
[0007] And the field where grown-in defects, such as FPD considered as the void reason to which hole type point defects gathered when a growth rate was a high speed comparatively with the above before and after 0.6 mm/min when these were classified according to the direction of the diameter of a crystal (field) as it was shown in drawing 6 for example, LSTD, and COP, exist in high density throughout the direction of the diameter of a crystal, and these defects exist is called the V-rich field (refer to the line (A) of drawing 5 , and drawing 6 (A)). Moreover, when a growth rate is 0.6 or less mm/min, the field where an OSF ring is generated from the circumference of a crystal, the defect of ratios of length to diameter (Large Dislocation: the code of the dislocation loop between grids, LSEPD, LFPD, etc.) considered to be dislocation loop reasons by the outside of this ring exists in a low consistency with lowering of a growth rate, and these defects exist is called the I-rich field (it may be called a ratio-of-length-to-diameter field). Furthermore, if a growth rate is made into a low

speed below 0.4 mm/min order, an OSF ring will condense and disappear at the core of a wafer, and the whole surface will serve as an I-rich field (the line (C) of drawing 5 , drawing 6 (C)).
[0008] Moreover, the existence of the field where neither FPD of a hole reason, LSTD, COP nor LSEPD of a dislocation loop reason and LFPD exist called N field to the outside of an OSF ring is discovered in the medium of a V-rich field and an I-rich field recently. It is reported that this field is the I-rich field side which is not so rich as there is almost no precipitation of oxygen by being in the outside of an OSF ring when oxygen precipitation heat treatment is performed and the contrast of a deposit is checked by X-ray observation etc., and LSEPD and LFPD are formed (refer to the line (B) of drawing 5 , and drawing 6 (B)).
[0009] And improve the temperature distribution in furnace of a pull-up machine for N field which exists only in the pole of a wafer part in the conventional CZ pull-up machine, and a pull-up rate is adjusted. V/G value (when setting a crystal pulling rate to V [mm/min] and setting the average of inclination to G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1300 degrees C]) If it controls to the whole wafer surface and a crystal overall length by setting to 0.20-0.22mm2 / **, and min the ratio expressed with V/G, and it is possible to extend N field all over a wafer, it has proposed (JP,8-330316,A).
[0010] However, if it is going to extend and manufacture such a super-low defective field into the whole crystal, since this field will be limited only to N field by the side of an I-rich field, if it is an experimental aircraft, it is [with a production machine, / precision control is difficult and / a difficulty] in productivity at any rate, and is not practical [a control range is very narrow on manufacture conditions, and].
[0011] When the present usual silicon single crystal, on the other hand, performs operation which changes a growth rate from a high speed to a low speed intentionally in a crystal orientation as shown in drawing 5 R> 5, As shown in drawing 6 , a whole (A) surface V-rich field mold, the coexistence mold of a (B) V-rich field and N-field, (C) A whole surface I-rich field mold (it may be called a ratio-of-length-to-diameter rich field mold), and a (D) V-rich field and an I-rich field coexistence mold (un-illustrating) are formed, and the growth rate of a crystal orientation is adjusted and manufactured so that each quality may be acquired according to the object application.
[0012] And the whole surface V-rich field mold of (A) is mass-produced as a reference standard among these. At a device process, although the V-N coexistence mold of (B) is manufactured as an amelioration article of (A), even if N-field is a high yield, it falls in a V-rich field and is imperfect. Although the whole surface I-rich field mold of (C) is manufactured as a particle monitor, ratio of length to diameter serves as a failure, and is not used as an object for device production. Moreover, even if it throws (A), (C), and the wafer of (D) each type into a device process, they have the inclination for the yield of a device to get worse, under the effect of a hole, the rearrangement between grids, etc. with the large size which remains on the wafer front face.
[0013] Although the whole surface N-field mold is proposed as a (E) type (un-illustrating) and the high yield was obtained recently on the whole surface, as it mentioned above, mass production nature of the actual condition is low. Furthermore, in a (B) and (E) type case, even if it heat-treats, in N-field by the side of I[in which oxygen does not deposit]-rich, gettering capacity may be insufficient and it is not necessarily stable. On the other hand, in the epitaxial wafer which uses a silicon single crystal wafer as a substrate, the deposit and a substrate with many defects are desired for the improvement in gettering capacity.
[0014]
[Problem(s) to be Solved by the Invention] It was made in view of such a trouble, when thermal oxidation processing is carried out, the nucleus of OSF or OSF is formed in the whole crystal surface or the whole surface except the periphery section, and this invention aims at obtaining the silicon single crystal wafer by the CZ process which has high gettering capacity under the stable manufacture condition.
[0015]
[Means for Solving the Problem] Invention which it was accomplished in order that this invention might attain said object, and was indicated to claim 1 of this invention is the silicon single crystal wafer raised by the Czochrlski method, and when it carries out thermal oxidation processing, it is a silicon single crystal wafer with which the nucleus of OSF or OSF exists in the whole crystal surface or the whole surface except the periphery section. Thus, the wafer of this invention became that whose gettering capacity improved remarkably by having formed OSF or its potential nucleus in the whole crystal surface or the whole surface except the periphery section.

[0016] And invention indicated to claim 2 of this invention is the silicon single crystal wafer raised by the Czochrlski method, and when it carries out thermal oxidation processing, it is a silicon single crystal wafer with which the nucleus of OSF or OSF exists in 90% or more of area of the whole wafer surface.
[0017] In this case, as indicated to claim 3, it is the silicon single crystal wafer indicated to claim 1 or claim 2, and is the silicon single crystal wafer with which FPD, COP, and ratio of length to diameter do not exist in the whole wafer surface.
[0018] Moreover, as indicated to claim 4, it is desirable that the oxygen densities of a wafer are under 24ppma (s) (ASTM'79 value). Although the nucleus of OSF exists when thermal oxidation processing is carried out if it does in this way, OSF serves as a silicon single crystal wafer with which it does not generate and FPD, COP, ratio of length to diameter, etc. do not exist in the whole wafer surface.
[0019] Furthermore, the consistency of OSF generated when said thermal oxidation processing is carried out, as indicated to claim 5 is 2 100 pieces/cm. It is the silicon single crystal wafer of the super-low defect in which it is the following. If it is an OSF consistency of this level, it will not have an adverse effect on the crystallinity of an epitaxial layer.
[0020] Invention indicated to claim 6 of this invention is the epitaxial wafer which used as the substrate the silicon single crystal wafer indicated to claim 1 thru/or claim 5, it is excellent in gettering capacity and gettering can fully realize it also with p mold substrate of high resistance.
[0021] and as the manufacture approach of such a silicon single crystal wafer [as indicated to claim 7 of this invention, when manufacturing a silicon single crystal with the Czochrlski method] The silicon single crystal raised sets the temperature gradient between 1400 degrees C to G (the amount of temperature changes / crystal orientation die length) [**/cm] from the melting point near [under crystal] the solid-liquid interface at the time of crystal growth. When the difference of the temperature gradient Gc of a crystal center part [**/cm] and the temperature gradient germanium of a crystal circumference part [**/cm] is expressed with **G= (germanium-Gc), so that **G may become 0 or negative In the defective distribution map in which having controlled whenever [furnace temperature / of the equipment to be used], and having set the axis of abscissa the axis of ordinate as the crystal diameter as the pull-up rate, and having shown defective distribution When an OSF field forms band-like reverse the mold of M characters or, and a U character mold, it is the manufacture approach of a silicon single crystal of pulling up a crystal, controlling within the limits of the pull-up rate corresponding to the minimum value of the inside line of an OSF field, and the pull-up rate corresponding to the maximum of the outside line of an OSF field.
[0022] The defective distribution map of drawing 1 which analyzed and searched for the result of an experiment and examination thus, to origin Whenever [furnace temperature / of the equipment used so that difference **G of the crystal center Of Inclination G and the crystal circumference may become 0 or negative from the melting point of silicon whenever / crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C] is controlled. If a crystal is pulled up controlling a pull-up rate within limits specified above The silicon single crystal with which the nucleus of OSF or OSF exists in the whole crystal surface or the whole surface except the periphery section when thermal oxidation processing like this invention is carried out, and defects, such as FPD, COP, and ratio of length to diameter, do not exist in the whole wafer surface is producible.
[0023] in this case, MCZ which impresses a magnetic field when manufacturing the silicon single crystal by said Czochrlski method, as indicated to claim 8 -- if law is used, it is stabilized more and a silicon single crystal can be manufactured. And if the magnetic field of 2000 or more Gausses is impressed in a horizontal magnetic field when manufacturing the silicon single crystal by said MCZ method as indicated especially to claim 9, stability will be acquired further.
[0024] Furthermore, as indicated to claim 10, it is desirable to make precision of the pull-up rate at the time of said crystal growth less than into the average**0.01 [mm/min] of the pull-up rate computed for every growth die length of 10cm of a crystal standard diameter portion (the body part of a single crystal is said). If precision of a pull-up rate is made into high degree of accuracy in this way, under the conditions easily specified by claim 7 thru/or claim 9, it is stabilized and a silicon single crystal can be manufactured.
[0025] Moreover, what is necessary is to prepare an annular solid-liquid interface heat insulator in pull-up equipment, and just to set spacing on this soffit and the front face of melt as 5-10cm, in order to control whenever [furnace temperature], as indicated to claim 11. If it carries out like this, difference **G= (germanium-Gc) of the temperature gradient Gc of the above-mentioned crystal center part [**/cm] and the

temperature gradient germanium of a crystal circumference part [**/cm] 0 or negative, That is, the temperature gradient of the crystal circumference and the temperature gradient of a crystal center can be equal, or whenever [furnace temperature] can be controlled so that the direction of the temperature gradient of the crystal circumference becomes lower than a crystal center, and OSF distribution can be used as band-like reverse the mold of M characters or, and a U character mold.

[0026] And the silicon single crystal wafer (claim 12) which slices the silicon single crystal manufactured by the manufacture approach of above-mentioned claim 7 thru/or a silicon single crystal according to claim 11, and is obtained can manufacture the epitaxial wafer excellent in gettering capacity, if an epitaxial layer is grown up by making this into a substrate.

[0027] Hereafter, although explained to a detail per this invention, this invention is not limited to these. In advance of explanation, lessons is taken from each vocabulary, and it explains beforehand. 1) K2 Cr 2O7 after cutting down a wafer from the silicon single crystal rod after growth and etching and removing a surface distortion layer with the mixed liquor of fluoric acid and a nitric acid in FPD (Flow Pattern Defect) A pit and a ripple pattern arise by etching a front face with the mixed liquor of fluoric acid and water (Secco etching). This ripple pattern is called FPD, and the defects of oxide-film pressure-proofing increase in number, so that the FPD consistency within a wafer side is high (refer to JP,4-192345,A).

[0028] 2) When the same Secco etching as FPD is performed, call SEPD (Secco Etch Pit Defect) a thing without FPD, a call, and a flow pattern for the thing accompanied by a flow pattern (flow pattern) with SEPD. When it is thought in this that large SEPD (LSEPD) 10 micrometers or more originates in a rearrangement cluster and a rearrangement cluster exists in a device, a current leaks through this rearrangement and it stops achieving the function as a P-N junction.

[0029] 3) Cut down a wafer from the silicon single crystal rod after growth, and carry out cleavage of the wafer to LSTD (Laser Scattering Tomography Defect) after etching and removing a surface distortion layer with the mixed liquor of fluoric acid and a nitric acid. Incidence of the infrared light can be carried out from this cleavage plane, and the scattered light by the defect which exists in a wafer can be detected by detecting the light which came out from the wafer front face. About the scatterer observed here, it is an institute etc., there is already a report, and it is regarded as the oxygen sludge (Jpn.J.Appl.Phys. Vol.32, P3679, 1993 reference). Moreover, the result that it is the void (hole) of octahedron is also reported by the latest research.

[0030] 4) the defect which becomes the cause of degrading oxide film pressure-proofing of the core of a wafer, with COP (Crystal Originated Particle) -- it is -- Secco -- by SC-1 washing (washing by the mixed liquor of NH4 OH:H2 O2:H2 O=1:1:10), the defect set to FPD if dirty works as a selection etching reagent, and is set to COP. The diameter of this pit is investigated with light scattering measurement by 1 micrometer or less.

[0031] 5) It is the defect which there are LSEPD, LFPD, etc. in ratio of length to diameter (Large Dislocation: code of the dislocation loop between grids), and is considered to be a dislocation loop reason. A large thing 10 micrometers or more is said that LSEPD described above also in SEPD. Moreover, also in FPD which LFPD described above, the magnitude of a head pit says a large thing 10 micrometers or more, and it is considered the dislocation loop reason also here.

[0032]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail, referring to a drawing. the place investigated in the detail about the boundary neighborhood of V field and an I region about the silicon single crystal growth by the CZ process as this invention persons proposed by Japanese Patent Application No. No. 199415 [nine to] previously -- **** of this boundary neighborhood -- the narrow field had few FPD(s), LSTD(s), and COP remarkably, and it discovered that there was a neutral field where ratio of length to diameter does not exist, either.

[0033] Then, if this neutral field can be extended all over a wafer, it will conceive that a point defect can be reduced substantially, and since the pull-up rate is almost fixed in the wafer side of a crystal, the main factors which determine concentration distribution of the point defect within a field will be temperature gradients in a growth (pull-up) rate and the relation of a temperature gradient. That a difference is in the temperature gradient of shaft orientations in a wafer side that is, on a problem If this difference can be reduced, that the concentration difference of the point defect within a wafer side can also be reduced A header, When controlling whenever [furnace temperature] and adjusting the pull-up rate so that the difference of the temperature gradient Gc of the crystal center section and the temperature gradient germanium of a crystal circumference part might be set to

**G=(germanium-Gc) <=5 degree-C/cm, a wafer without the defect which the whole wafer surface becomes from N field came to be obtained.

[0034] In this invention, as a result of having used the crystal pulling equipment by the small CZ process, difference **G of the above temperature gradients rearranging the structure in a furnace, changing **G, changing a pull-up rate and investigating the inside of the crystal face, the following knowledge was newly acquired. Spacing from the surface of hot water to the soffit of an annular solid-liquid interface heat insulator is change, **G was changed, to 0.6 - 0.3 mm/min, it slows down 0.05 mm/min of average pull-up rates of a single crystal standard diameter portion at a time, they were changed every 10cm, the OSF ring disappeared focusing on crystal bulk, and the structure in a furnace of the used equipment investigated signs that a ratio of length to diameter field was formed, as showed in drawing 4 (a).

[0035] The result was analyzed and it was shown in drawing 1 as a defective distribution map. An axis of abscissa is the crystal diameter direction, and an axis of ordinate is a growth rate. When the temperature gradient germanium of the 0 or negative, i.e., crystal, circumference and the temperature gradient Gc of a crystal center have equal **G or the temperature gradient germanium of drawing 1 of the crystal circumference is lower than the temperature gradient Gc of a crystal center, in the range of 0.48 - 0.45 mm/min, OSF of a growth rate is beltlike, and it means being distributed over the reverse mold of M characters or, and the U character mold. And when a growth rate looks at the range of 0.47 - 0.45 mm/min as the crystal face among this distribution, it turns out that 90% or more of area except the periphery section (N-field by the side of I-rich) serves as a wafer with which OSF or its potential nucleus exists in the OSF field like drawing 3 (a).

[0036] And the pull-up rate corresponding to the minimum value of the inside line of an OSF field when, as for this invention, an OSF field forms band-like reverse the mold of M characters or, and a U character mold in the defective distribution map of drawing 1 , It is a thing called the method of a pull-up in a crystal, controlling a pull-up rate within the limits of the pull-up rate corresponding to the maximum of the outside line of an OSF field. If it says concretely in the above-mentioned example, a growth rate will be set up within the limits of 0.47 - 0.45 mm/min, and it will control and pull up to high degree of accuracy so that it may become less than **0.01 mm/min of averages of the target growth rate computed for every growth die length of 10cm of a crystal standard diameter portion. In this way, the obtained single crystal rod was made into vertical division, and defective distribution was investigated like the above. The result is shown in drawing 2 . The overall length is covered, an OSF field is distributed in the shape of a cylinder, and, as for the part which maintained and pulled up the optimal growth rate so that clearly from drawing 2 , it turns out that the periphery sections other than an OSF field are N-fields by the side of I-rich.

[0037] Drawing 3 (b) expresses the wafer which sliced [carried out grinding, removed it and] and obtained the OSF non-generated field of the periphery of the single crystal rod obtained in this way (N-field), and is a silicon single crystal wafer with which OSF or its potential nucleus exists to 100% in a field.

[0038] **G exceeds 0. Conversely, in plus (i.e., when the temperature gradient germanium of the crystal circumference is higher than the temperature gradient Gc of a crystal center) Even if OSF is beltlike and it is distributed over the shuttle-race-back mold, as the growth rate showed the range of about 0.6 to 0.4 mm/min to drawing 5 , and it sees with the crystal-face interior division cloth of drawing 6 , the whole surface or the whole surface except the periphery section is an OSF field like this invention article. It turns out that the wafer with which OSF or its potential nucleus existed in a large area called 90% or more of whole wafer surface, and the periphery section was formed in N-field by the side of I-rich does not appear. The above thing is not discovered when the conventional **G experiments on a plus side with large crystal pulling equipment, but as a result of investigating the crystal with which the **G above-mentioned this time used 0 or negative crystal pulling equipment, it is discovered.

[0039] About whenever [furnace temperature / of the pull-up equipment in this examination], as a result of analyzing wholeheartedly using the comprehensive heat transfer analysis software FEMAG (F. 33 Dupret, P.Nicodeme, Y.Ryckmans, P.Wouters, and M.J.Crochet, Int.J.HeatMass Transfer, 1849 (1990)), it becomes clear.

[0040] It turns out that OSF is not generated by thermal oxidation processing and a device is not affected on the other hand about OSF which exists in the wafer of this invention even if the nucleus of OSF exists when it considers as hypoxia concentration in the whole wafer surface from the latest research. The threshold value of this oxygen density is an OSF consistency 100 pieces/cm, when the oxygen densities in the whole wafer surface

were under 24ppma(s) (ASTM'79) and thermal oxidation processing of a wafer is performed, as a result of using the same crystal pulling equipment and pulling up the crystal of some kinds of oxygen density level 2 That it can control below or not generating were checked.
[0041] That is, although it is to 24ppma(s) that according to examination the nucleus which serves as OSF covering a crystal overall length exists when an oxygen density is gradually lowered while raising the crystal of one, but OSF is observed when thermal oxidation processing of a wafer is performed and the nucleus of OSF existed in less than 24 ppmas, it turned out that OSF by thermal oxidation processing is not generated.
[0042] Incidentally, in order to set the oxygen density under growth crystal to less than 24 ppmas, that what is necessary is just to carry out by the approach generally used from the former, distribution etc. can be adjusted whenever [rotational frequency / of a crucible /, or melt internal temperature], and the means of controlling the convection current of melt can perform easily.
[0043] In addition, the consistency of OSF generated when thermal oxidation processing of the wafer produced by this invention is carried out is 2 100 pieces/cm. When it is a low defect very much, it was an OSF consistency of this level and it considers as an epitaxial wafer the following, it does not have an adverse effect on the crystallinity of an epitaxial layer. In this case, with light (Wright) liquid, selective etching processing was carried out and measurement of an OSF consistency measured to it, after performing heat treatment for 1200 degrees C / 100 minutes to the silicon single crystal wafer.
[0044] Hereafter, drawing 4 (a) explains the example of a configuration of the crystal pulling equipment by the CZ process used by this invention. As shown in drawing 4 R> 4 (a), this crystal pulling equipment 30 The pull-up room 31, the crucible 32 prepared all over the pull-up room 31, and the heater 34 arranged around a crucible 32, It has the reel style (not shown) which rotates or rolls round the crucible maintenance shaft 33 made to rotate a crucible 32 and its rolling mechanism (not shown), the seed chuck 6 holding the seed crystal 5 of silicon, the wire 7 that pulls up a seed chuck 6, and a wire 7, and is constituted. A quartz crucible is prepared in the side in which a crucible 32 holds the silicon melt (molten bath) 2 of the inside, and the graphite crucible is prepared in the outside. Moreover, the heat insulator 35 is arranged around [outside] the heater 34.
[0045] Moreover, in order to set up the manufacture conditions in connection with the manufacture approach of this invention, the annular solid-liquid interface heat insulator 8 is formed in the periphery of the solid-liquid interface 4 of a crystal. This solid-liquid interface heat insulator 8 forms the spacing 10 of 5-10cm between that soffit and surface of hot water 3 of silicon melt 2, and is installed in it. The up heat insulator 9 prepared on the heat insulator 35 which surrounds the heater shown in drawing 4 (b) will be used according to conditions whenever [furnace temperature], and spacing 10 will be adjusted in that case. Furthermore, coolant gas may be sprayed or the tubed cooling system (un-illustrating) which interrupts radiant heat and cools a single crystal may be formed. Independently, by installing the magnet which is not illustrated in the horizontal outside of the pull-up room 31, and impressing magnetic fields, such as a horizontal direction or a perpendicular direction, to silicon melt 2, the convection current of melt is controlled and, recently, the so-called MCZ method for measuring the stable growth of a single crystal is used in many cases.
[0046] Next, the single-crystal-growth approach by above crystal pulling equipment 30 is explained. First, within a crucible 32, the high grade polycrystal raw material of silicon is heated more than the melting point (about 1420-degreeC), and is dissolved. Next, the head of seed crystal 5 is made contacted or immersed in the surface abbreviation core of melt 2 by beginning to roll a wire 7. Then, while rotating the crucible maintenance shaft 33 in the proper direction, single crystal growth is started by rolling round rotating a wire 7 and pulling up seed crystal 5. Henceforth, the single crystal rod 1 of an approximate circle column configuration can be obtained by adjusting a pull-up rate and temperature appropriately.
[0047] In this invention, that in this case, it is important especially in order to attain the object of this invention As shown in drawing 4 (a) or drawing 4 R> 4 (b), it sets to the periphery space of the liquefied part in the single crystal rod 1 on the surface of hot water of the pull-up room 31. It is having formed the annular solid-liquid interface heat insulator 8 so that the temperature region from the melting point of the crystal near the surface of hot water to 1400 degrees C could be controlled, and having arranged the up heat insulator 9 on a heat insulator 35.
[0048] Namely, what is necessary is to form the annular solid-liquid interface heat insulator 8 in the pull-up room 31, and just to set the spacing 10 on this soffit and the front face of melt as 5-10cm, as shown in drawing 4 (a) in order to control whenever [this furnace temperature]. If it carries out like this, the temperature gradient

of the 0 or negative, i.e., crystal, circumference and the temperature gradient of a crystal center have equal difference **G= (germanium-Gc) of the temperature gradient Gc of the above-mentioned crystal center part [**/cm], and the temperature gradient germanium of a crystal circumference part [**/cm], or whenever [furnace temperature] can be controlled so that the direction of the temperature gradient of the crystal circumference becomes lower than a crystal center. As shown in drawing 4 (b), while adjusting the above-mentioned spacing 10 as an option, there is also the approach of adding the up heat-insulating element 9 on a heat insulator 35, and controlling the heat dissipation from up space.
[0049] moreover, about the precision of the pull-up rate at the time of said crystal growth If it is desirable to carry out to less than the average**0.01 of the pull-up rate computed for every growth die length of 10cm of a crystal standard diameter portion [mm/min] and the precision of a pull-up rate is in this range It is stabilized and the silicon single crystal to which a crystal overall length is covered and cylinder-like an OSF field or its potential nucleus exists to 90% or more in a field according to the synergistic effect of whenever [above-mentioned furnace temperature], (**G) and a pull-up rate condition value can be manufactured.
[0050] When the silicon single crystal wafer which slices the silicon single crystal manufactured by the manufacture approach of the silicon single crystal described above , and is obtain carries out thermal oxidation processing to a wafer , since gettering capacity improves remarkably by form the nucleus of OSF or OSF in the whole crystal surface or the whole surface except the periphery section and FPD , COP , and ratio of length to diameter do not exist in the whole wafer surface , oxide film pressure-proofing is also a good super-low defective article . And the consistency of OSF which will be generated when thermal oxidation processing is carried out if hypoxia-ization is used together is 2 100 pieces/cm. It becomes the following low consistencies, and the silicon single crystal wafer which has gettering capacity can be manufactured as a substrate of an epitaxial wafer, without having an adverse effect on an epitaxial layer.
[0051]
[Example] Hereafter, although the example of this invention is given and explained, this invention is not limited to these.
(Example 1) With the pull-up equipment 30 shown in drawing 4 (a), 100kg of raw material polycrystalline silicon was charged to the 24 inch quartz crucible, and the silicon single crystal rod with the diameter of 8 inches, a bearing <100>, and a body die length of about 1m was pulled up. The used structure in a furnace (hot zone: HZ) set the spacing 10 of the surface of hot water 3 and the soffit of the annular solid-liquid interface heat insulator 8 as 60mm, and held the water temperature of silicon melt 2 at about 1420 degrees C. And the horizontal magnetic field of 3000Gauss(es) was impressed as a magnetic field in this case.
[0052] Under the above conditions, it slows down 0.05 mm/min of average pull-up rates at a time, they were changed every 10cm, to 0.6 - 0.3 mm/min, OSF disappeared focusing on crystal bulk, and signs that a ratio-of-length-to-diameter field was formed were investigated. The search procedure made the crystal 2mm in thickness at vertical division, carried out etching clearance of the processing distortion of a front face, and produced the sample of two sheets. One sheet observed FPD and ratio of length to diameter, after performing SEKO etching during 30 minutes. Moreover, about the one remaining sheets, after performing heat treatment for 1200 degrees C / 100 minutes, selective etching processing was carried out with the Wright reagent, and the generating situation of OSF was checked. The result was collectively shown in drawing 1 as a defective distribution map. An axis of abscissa is the crystal diameter direction, and an axis of ordinate is a pull-up rate. Drawing to OSF is beltlike and it turns out that it is distributed over the reverse mold of M characters or, and the U character mold. When this is seen, in order to obtain this invention article, with the structure in this furnace, it turns out that what is necessary is just to control a growth rate to 0.47 - 0.45 mm/min.
[0053] Next, in order to expand this invention article whose whole surface within the crystal face is an OSF field to a crystal orientation based on the above-mentioned examination and experimental result, it was set as the optimal growth rate (0.47 - 0.45 mm/min), and it controlled and pulled up so that it might become the less than **0.01 averages of the target growth rate computed for every growth die length of 10cm of a crystal standard diameter portion. In this way, the obtained single crystal rod was made into vertical division, and ****** was investigated like the above. The result is shown in drawing 2 R> 2. The overall length is covered, an OSF field is distributed in the shape of a cylinder, and, as for the part which maintained and pulled up the optimal growth rate so that clearly from drawing, it turns out that peripheries other than an OSF field are N-fields by the side of I-rich.

[0054] The single crystal rod was independently processed into the pull-up and the mirror-polishing finishing wafer on the above and these conditions, and assessment of FPD, ratio of length to diameter, and OSF was performed. Consequently, it was distributed circularly and OSF as shown in drawing 3 (a) was 95% of wafer whose peripheries other than an OSF field are N-fields by the side of I-rich. And FPD and ratio of length to diameter were not observed. In addition, the oxide-film proof-pressure property of this wafer became 100% at the rate of C-mode excellent article. The C-mode Measuring condition is as follows.
1) Oxide-film thickness : 25nm Two measuring electrode: Phosphorus dope polish recon and 3 electrode-surface product:8mm2 4 judging current: 1 mA/cm2, five seals Law: Dielectric-breakdown electric field judged the thing of 8 or more MV/cm to be an excellent article.
[0055] (Example 2) As shown in drawing 4 (b), the up heat insulator 9 was installed for the structure in a furnace on the heat insulator 35, and except having set spacing 10 of the silicon melt side 3 and the soffit of the annular solid-liquid interface heat insulator 8 to 50mm, as a result of pulling up on the same conditions as an example 1, the single crystal rod of the almost same quality as an example 1 was obtained.
[0056] (Example 3) the consistency of OSF [in / when an example 1 and these conditions estimated the pull-up and the defect except having held down the oxygen density under growth crystal to 24 or less ppmas / an OSF field] -- an average of [0-10 piece/cm2 and] -- about 2 -- piece/cm2 it is -- it is a low consistency very much and was hardly observed.
[0057] (Example 4) Epitaxial growth was performed using the silicon substrate obtained in the example of this invention. The epitaxial layer was grown up by the approach usually performed on the substrate produced in the example 1. And although selective etching processing according the front face of an epitaxial layer to a Wright reagent was performed and observed, crystal defects, such as SF (a stacking fault, Stacking Fault), were not observed at all, but were very good epitaxial wafers.
[0058] In addition, this invention is not limited to the above-mentioned operation gestalt. The above-mentioned operation gestalt is instantiation, and no matter it may be what thing which has the same configuration substantially with the technical thought indicated by the claim of this invention, and does the same operation effectiveness so, it is included by the technical range of this invention.
[0059] For example, in the above-mentioned operation gestalt, although the example was given and explained per when a silicon single crystal with a diameter of 8 inches was raised, this invention is not limited to this but can be applied also to the diameter of 10-16 inches, or the silicon single crystal beyond it. Moreover, it cannot be overemphasized that this invention is applicable also to the so-called MCZ method for impressing a level magnetic field and length magnetic field, a cusp field, etc. to silicon melt.
[0060]
[Effect of the Invention] As explained above, when thermal oxidation processing is carried out according to this invention, the wafer with which gettering capacity improves remarkably and FPD, COP, and ratio of length to diameter do not exist in the whole wafer surface can be easily produced by the high yield by forming the nucleus of OSF or OSF in the whole crystal surface or the whole surface except the periphery section. And if hypoxia-ization is used together, OSF also serves as a low consistency and the silicon single crystal wafer which has gettering capacity as a substrate of an epitaxial wafer can be manufactured.

[Translation done.]

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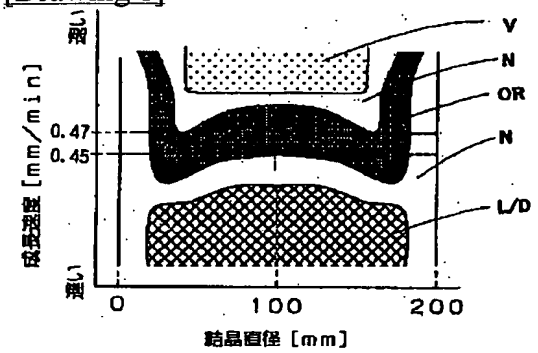
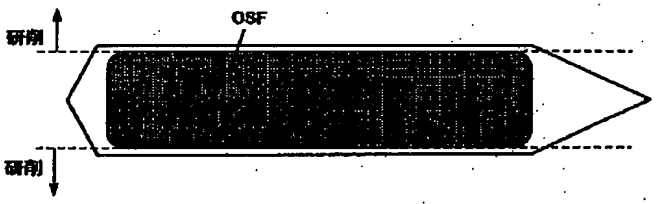
DRAWINGS

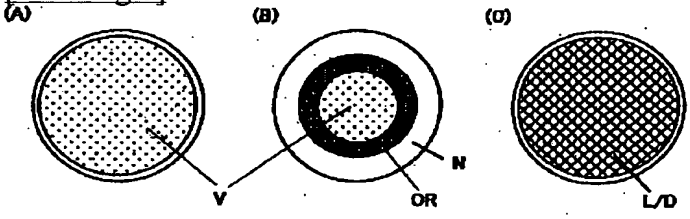
[Drawing 1]



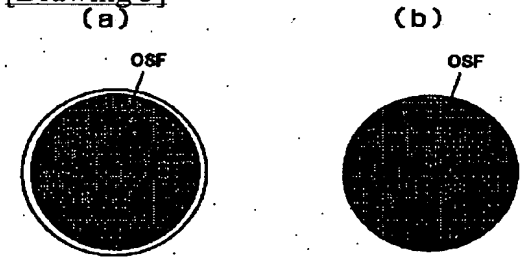
[Drawing 2]



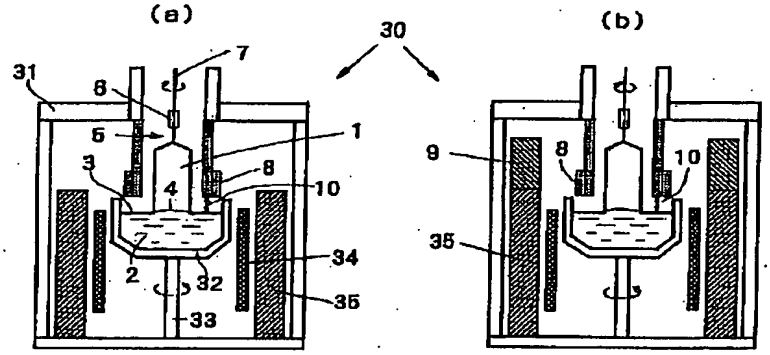
[Drawing 6]



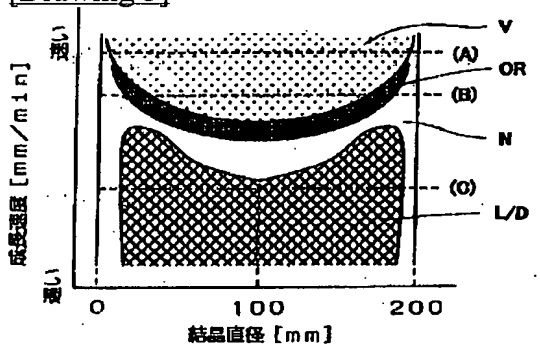
[Drawing 3]



[Drawing 4]



[Drawing 5]



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